09/480 223

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

: 6,835,627 B1

Page 1 of 2

DATED

: December 28, 2004

INVENTOR(S) : Seamus Paul Whiston et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

### Column 1,

Line 16, should read -- devices as well as bipolar CMOS (BiCMOS) devices on the -- Line 34, should read -- be appropriately aligned with the gate of LDMOS device, -- Line 36, should read -- Tilt Implant in 0.6 µm BCD5 Process, Flash Memory --

## Column 3,

Line 60, should read -- In one embodiment of the invention the DMOS device is --

### Column 4,

Line 6, should read -- conventional CMOS or BiCMOS process, and thus, LDN- -- Line 61, should read -- invention. An N-well 4 for the LDNMOS 1 and a P-well 5 --

## Column 5,

Line 14, should read -- respectively, beneath the gates 14 by implanting appropriate -- Line 28, should read -- the dopant is directed into the N-well 4 in the direction of the -- Line 44, should read --  $\alpha$  by setting the tilt angle of implant at a first tilt angle  $\theta$  of -- Line 46, should read -- at the second angle  $\beta$  by setting the tilt angle of implant at --

## Column 6,

Line 5, should read --  $\theta$  of 45° for determining the drain/source threshold voltage -- Line 7, should read -- implanted in the P-well 5 at the second angle  $\beta$  of 83° using -- Line 47, should read -- be formed on the wafer either simultaneously or sequentially -- Line 49, should read -- LDMOS devices have been described as being formed using -- Line 55, should read -- P-body region has been described as being implanted before -- Line 56, should read -- N-body region, it will be appreciated that the P-body and -- Line 57, should read -- N-body regions may beformed in any order. --

#### Column 7.

Line 27, should read -- 7. A method as claimed in claim 6 in which the second --

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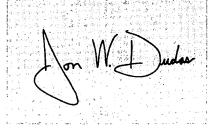
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

## Column 8,

Line 4, should read -- implanted in each of steps (a) and (b) may be the same or --

Signed and Sealed this

Seventh Day of June, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office